

## REMARKS

Applicant thanks the Examiner for the continuing attention to this application.

As to the objection to the Abstract and the rejection of Claims 1-21 under 35 U.S.C.

§ 112, Applicant refers the examiner to the following paragraph from the specification:

**[0024]** In specific embodiments, the present invention involves using two non-contiguous (or “separated”) bit areas to store real numbers. These areas are referred to as non-contiguous because there is no automatic binary carry in either direction with regard to the bit areas. Furthermore, these areas are referred to as non-contiguous because unlike other encoding schemes, in a given number there is no dependency on either part of the number to determine the value of the other part. In other words, the integer portion of a decimal is dependent only on the integer portion of the stored binary value. Likewise, the fractional portion of a decimal is dependent only on the fractional portion of the stored binary value. In terms of their actual storage in a computer’s memory, however, the different portions of the numbers may be stored in memory locations next to each other. Thus, according to specific embodiments of the invention, a real number as discussed herein is stored as an integer part (IP) and a fractional part (FP).

Thus, the specification provides a clear definition of the term in question in terms that would be understood to anyone of ordinary skill in the computer art. To repeat, according to the invention and the specification definition, the term non-contiguous as used in this application indicates (1) there is no automatic binary carry in either direction with regard to the bit areas; and (2) for a given number there is no dependency on either part of the number to determine the value of the other part. In other words, the integer portion of a decimal is dependent only on the integer portion of the stored binary value. Likewise, the fractional portion of a decimal is dependent only on the fractional portion of the stored binary value.

However, as the specification states, in terms of their actual storage in a computer’s memory, however, the different portions of the numbers may be stored in memory locations next to each other.

### **Yuval**

Applicant traverses the Examiner’s characterization of Yuval. According to the specification of Yuval, “FIG. 3b illustrates the bit-wise breakdown in accordance with IEEE 32-bit floating point data representations 12. The least significant twenty-three bits (22-0) represent

the significand. The next eight bits (23-30) represent the exponent and the most significant bit (31) represents the sign." Nothing in Yuval suggests that there is a separate integer part (IP) and a fractional part (FP). In fact, what Yuval states is:

[0007] Conversions from the native floating point values into 16-bit floating point values must properly convert a sign, exponent, and significand of the native floating point value into a corresponding 16-bit floating point representation. Conversion of the sign is rather straight forward. The sign bit may be simply copied over to the 16-bit floating point representation. As for the magnitude of the number, the native floating point should map to the 16-bit floating point value that is closest to the native floating point value. Hence, the native floating point number is "rounded" to the nearest 16-bit floating point value. This may be accomplished by considering four ranges of the native floating point values. First, ranges above the maximum representable 16-bit floating point value are generally treated as infinite and clamped to a value representing infinity in the 16-bit floating point representation. Second, values that round to below the smallest 16-bit floating point representation may be clamped. Third, values must be rounded for normalized or denormalized 16-bit floating point values.

Thus, Yuval is directed to converting from one standard floating point representation to another floating point representation. Nothing in Yuval suggests having separate IP and FP with no automatic carry.

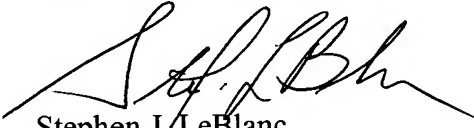
Likewise, Pangal does not discuss a separate IP and FP with no automatic carry between them.

In light of these remarks, the rejection claims should be withdrawn. Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If after consideration of the above response, the Examiner does not find that all pending claims are in condition for allowance, **applicant hereby requests a telephone interview with the Examiner.**

**Please contact the undersigned at (510) 769-3508.**

QUINE INTELLECTUAL PROPERTY LAW GROUP, P.C.  
P.O. BOX 458  
Alameda, CA 94501  
Tel: 510 337-7871  
Fax: 510 337-7877

Respectfully submitted,

  
Stephen J. LeBlanc  
Reg. No. 36,579

Attachments:

- 1) A transmittal sheet;
- 2) A receipt indication postcard